IN THE UNITED STATES PATENT OFFICE

Applicant:

Tao Pi et al.

Assignee:

Xilinx, Inc.

Title:

"FPGA Lookup Table with Transmission Gate

Structure for Reliable Low-Voltage Operation"

Serial No.:

Not Yet Known

File Date:

10-24-03

Examiner:

Not Yet Known

Art Unit:

Not Yet Known

Divisional of

Serial No.:

10/241,094

File Date: 09-10-02

Docket No.:

X-1128-1D US

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Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the two (2) references listed in the attached Substitute for Form PTO-1449 (Information Disclosure Statement by Applicant).

All of these references were cited in prior related U.S. patent application Serial Number 10/241,094 filed September 10, 2002 to which this application claims priority. Copies of these references have not been supplied herein since they were previously submitted in the parent case.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully Submitted,

Lois D. Cartier Agent for Applicants

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Substitute for form 1449A/PTO				Complete if Known		
Substitute	101 101111 1449701	10		Application / Conf. No.	Unknown /	
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STAT	STATEMENT BY APPLICANT			First Named Inventor	Tao Pi	
01711				Art Unit	Unknown	
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Sheet	1	of	2	Attorney Docket Number	X-1128-1D US	

	U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No.¹	Document Number Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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	FOREIGN PATENT DOCUMENTS								
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Initials *	Initials * No.1	Country Code ³ -Number ⁴ -Kind Code ⁵ (<i>if known</i>)	MM-DD-YYYY	Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear				

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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁵ Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (10-01)
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Sheet	2	of	2	Attorney Docket Number	X-1128-1D US	

OTHER NON PATENT LITERATURE DOCUMENTS						
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
		Xilinx, Inc.; "Virtex-II Platform FPGA Handbook"; published December 2000, available from Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124; pp. 33-75.				
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